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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/893,455	06/29/2001	Hiroyuki Nishi	SKI.007D	7179

7590

05/21/2003

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RESTON, VA 20191

EXAMINER

ORTIZ, ANGELA Y

ART UNIT	PAPER NUMBER
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1732

5

DATE MAILED: 05/21/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

AS-5

Office Action Summary

Application No.

09/893,455

Applicant(s)

NISHI ET AL.

Examiner

Angela Ortiz

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 03 April 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 7-12 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 7-12 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 29 June 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☒ Certified copies of the priority documents have been received in Application No. 09/265,841.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2.
- 4) ☐ Interview Summary (PTO-413) Paper No(s) _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of claims 7-12 in Paper No. 4 is acknowledged.

Drawings

Figures 7 and 8 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The words "APPARATUS AND" should be deleted from the title.

Claim Objections

Claim 8 is objected to under 37 CFR 1.75 as being a substantial duplicate of claim 7. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is

proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

Applicant is advised that should claim 7 or 8 be found allowable, claim 8 or 7 will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

Applicant correctly argued in the amendment filed 03 April 2003, that a double patenting *rejection* was not appropriate as duplicate claims in the same application are not the basis for statutory or non-statutory double patenting.

Please note that a claim warning is appropriate until one of the claims is found allowable. This will give the applicant an opportunity to correct the problem and avoid a later objection. Upon allowance of one claim, the other claim will be objected to as a duplicate under 37 CFR 1.75. Note that duplicate claim warning/objections are categorized with the subject of double patenting, although they are from different subsections of the MPEP.

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The claims have been duplicated in an attachment for the benefit of the applicant, so that the similarity can be noted. Applicant previously argued that the preambles are different for each claim; however, in the claims of record, the preambles do not differ.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 7, 8 and 12 are rejected under 35 U.S.C. 102(e) as being anticipated by Weber, USP 6,495,083.

The cited reference teaches the claimed method of manufacturing semiconductor devices including placing semiconductor mounted devices (12,14) within the cavity of a transfer mold having a top half (32) and a bottom half (34). During the molding process, as fluent resin reaches a desired level during filling of the cavity, the mold cavity pressure is controlled by the mold vent (46) by allowing excess to flow into cavity (42) so that a predetermined threshold pressure is not reached. Note that the claimed semiconductor chip is an integrated chip, and the claimed lead frame is a substrate. See col. 4, lines 28-67; col. 5, lines 1-35.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 9-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsuzuku et al., USP 4,426,341 in view of Saeki et al., USP 4,954,301.

The cited primary reference substantially teaches the basic claimed method including transfer molding semiconductor devices using control means for optimizing the molding parameters. A predetermined pressure level is set prior to the initiation of the transfer molding operation. Movement of the plunger downward is initiated to force resin into the molding cavity. As the filling of the resin within the mold cavity progresses, the displacement of the plunger and the resin pressure inside the cavity is

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monitored by control means including a pressure sensor. When the maximum pressure is reached, the plunger is retracted and the relief valve opens. See col. 4, line 50 to col. 5, line 25; col. 5, line 37 to col. 6, line 36.

The cited primary reference does not set forth the claimed feature of determining the specified amount of resin in the mold cavity using distance and time traveled by the plunger.

The added reference teaches as conventional the molding process as claimed including the feature of measuring the distance traveled by the plunger to determine the fullness of the molding cavity. By measuring time and distance as an initial reference, transfer molding is performed as the plunger is moved downward at a desired velocity for a set amount of time and distance, the velocity is reduced after a desired period and then continued to fill the cavity. This prevents the plunger from impinging against the resin tablet at a high velocity to form voids in the molding resin even when the velocity is changed during different molding conditions. See col. 3, lines 39-45, 65-68; col. 4, lines 1-10, 40-68; col. 5, lines 1-10, 55-60; col. 6, lines 27-55.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include plunger displacement and travel time means as set forth in the added reference, when performing the process set forth in the primary reference, as the displacement and time means prevent the plunger from impinging against the resin tablet and creating voids or air pockets within the molding resin.

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With respect to claim 9, note that the mold set forth in the primary reference is not completely filled when the pressure is determined and is deemed readable on the claimed level "of about half", see col. 5, lines 55-60.

Allowable Subject Matter

The following claim has been drafted by the examiner and considered to distinguish patentably over the art of record in this application:

A method for manufacturing semiconductor device packages comprising the steps of:

providing a transfer molding apparatus including a top-half mold and a bottom-half mold that forms a cavity as a molding space for a package, a transfer pot as a resin loading space, a plunger that communicates with the transfer pot to force resin out of the pot and into the mold cavity;

placing a lead frame having a semiconductor element mounted thereon between the top-half mold and the bottom-half mold within the cavity;

introducing resin into the mold cavity using the plunger, and forming the semiconductor device package; and

reducing a pressure in the cavity formed by the top-half mold and the bottom-half mold, using a pressure adjuster to extract air from the cavity when a specified amount of resin has been supplied to the cavity.


Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. USP's 3741700; 3836303; 4038004; 4900485; 5454991; 5626887; 5690885; 6267577; 6444035; 6495083.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Angela Ortiz whose telephone number is 703-308-4446. The examiner can normally be reached on Monday-Thursday 9:00-6:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Crispino can be reached on 703-308-3853. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9310 for regular communications and 703-872-9311 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0661.


Angela Ortiz
Primary Examiner
Art Unit 1732

ao
May 16, 2003

5 7/ A method for manufacturing semiconductor devices comprising the steps of:

placing a semiconductor-element-mounted lead frame between a top-half mold and a bottom-half mold; and

reducing the pressure in a cavity formed by said top-half mold and said
10 bottom-half mold when a specified amount of resin has been supplied into said cavity.

--8. A method for manufacturing semiconductor devices, comprising:

placing a lead frame having a semiconductor element mounted thereon,
between a top-half mold and a bottom-half mold; and

reducing a pressure in a cavity formed by the top-half mold and the bottom-half
mold when a specified amount of resin has been supplied into the cavity.